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<u>L3</u>	L1 and ((selectively near5 connect\$3) same first same second)	24	<u>L3</u>
<u>L2</u>	L1 and (selectively near5 connect\$3)	162	<u>L2</u>
<u>L1</u>	(serial adj1 parallel) near10 port	4210	<u>L1</u>

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<u>L3</u>	L1 and ((selectively near5 connect\$3) same first same second)	24	<u>L3</u>
<u>L2</u>	L1 and (selectively near5 connect\$3)	162	<u>L2</u>
<u>L1</u>	(serial adj1 parallel) near10 port	4210	<u>L1</u>

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Search Results -

Terms	Documents
L1 and ((selectively near5 connect\$3) same first same second)	0

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L5 L1 and ((selectively near5 connect\$3) same first same second)

0 L5

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L4 L1 same ((selectively near5 connect\$3) same first same second)

1 L4

L3 L1 and ((selectively near5 connect\$3) same first same second)

24 L3

L2 L1 and (selectively near5 connect\$3)

162 L2

L1 (serial adj1 parallel) near10 port

4210 L1

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EAST - [Untitled1:1]

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Drafts

- BRS:
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- Active**
 - L1: (244) (serial adj1
 - L2: (0) l1 same (select
 - L3: (0) l1 same selecti
 - L4: (1) l1 same selecti
 - L5: (8) l1 and (selecti
- Failed
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- Tagged (0)
- UDC
- Queue
- Trash

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☒ Plurals
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1	BRS	L1	244	(serial adj1 parallel) same "seria	USPA T	2005/09/2 9 15:31				
2	BRS	L2	0	l1 same (selectively near5 connect\$3)	USPA T	2005/09/2 9 15:31				
3	BRS	L3	0	l1 same selectively same connect\$3	USPA T	2005/09/2 9 15:30				
4	BRS	L4	1	l1 same selectively	USPA T	2005/09/2 9 15:30				
5	BRS	L5	6	l1 and (selectively near5 connect\$3)	USPA T	2005/09/2 9 15:31				

EAST - [Untitled1:1]

File View Edit Tools Window Help

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11 and (selectively near5 connect53)

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2	<input type="checkbox"/>	<input type="checkbox"/>	US 6230078	20010508	16	Simplified animatronic and CNC svstem	700/247	710/63
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6195359	20010227	16	Intelligent router for remote internet access	370/401	370/465;
4	<input type="checkbox"/>	<input type="checkbox"/>	US 5867406	19990202	25	Docking device for a portable computer and a	708/140	375/222
5	<input type="checkbox"/>	<input type="checkbox"/>	US 5819112	19981006	20	Apparatus for controlling an I/O port	710/36	361/683;
6	<input type="checkbox"/>	<input type="checkbox"/>	US 5471585	19951128	10	Personal computer svstem with input/output	710/5	361/729;
7	<input type="checkbox"/>	<input type="checkbox"/>	US 4897662	19900130	41	Integrated circuit with wireless freshness seal	710/13;	710/107;
8	<input type="checkbox"/>	<input type="checkbox"/>	US 4744006	19880510	19	Apparatus for expanding the input/output capabi	710/263;	710/306;
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Lowry, M.E.;
Selected Topics in Quantum Electronics, IEEE Journal of
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Volume 26, Issue 4, April 1991 Page(s):549 - 554
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Schroeder, M.D.; Birrell, A.D.; Burrows, M.; Murray, H.; Needham, R.M.; Rodeheffer, T.L.; Satterthwaite, E.H.; Thacker, C.P.;
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5-7 Feb. 2003 Page(s):165 - 172
Digital Object Identifier 10.1109/EMPDP.2003.1183583

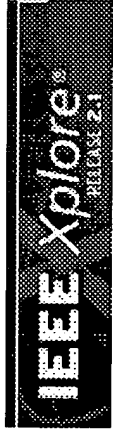
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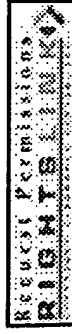
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A high speed dual port memory with simultaneous serial and random mode access for video applications

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Publication Date: Dec 1984

Volume: 19, Issue: 6

On page(s): 999 - 1007

ISSN: 0018-9200

Posted online: 2003-01-06 16:59:32.0

Abstract

A 64K/spl times/1 NMOS dynamic RAM which is interfaced in an on-chip 256-bit high-speed shift register is described. The device allows parallel transfer of 256 bits from a selected row in memory to the shift register in a normal RAS cycle time. Subsequently, the device provides simultaneous and asynchronous access from both the DRAM and the serial ports. The shift register can operate at a typical frequency of 33 MHz. When used in conjunction with multiple devices of the same design, a high-resolution bit-mapped video display system can be achieved with video bandwidths beyond 100 MHz. The dual-ported nature of the device allows a graphics processor to operate on the DRAM portion of the device while the shift register simultaneously provides a video data stream to a video display system.

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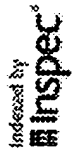
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